

L Number	Hits	Search Text	DB	Time stamp
-	476	((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:39
-	12890	((integrated adj1 circuit) or VLSI or LSI or IC) same layout	USPAT; EPO; JPO; DERWENT	2003/05/13 10:41
-	13063	((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout )	USPAT; EPO; JPO; DERWENT	2003/05/13 10:41
-	19807	((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin)	USPAT; EPO; JPO; DERWENT	2003/05/13 10:49
-	474	((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout ) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:47
-	4550	716/\$.ccls.	USPAT; EPO; JPO; DERWENT	2003/05/13 10:47
-	78	((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout ) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))) and 716/\$.ccls.	USPAT; EPO; JPO; DERWENT	2003/05/13 10:47
-	421	((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout ) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin)))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:52
-	52	716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout ) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:53
-	32	optimiz\$5 and (716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout ) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:55

-	18	(logic\$4 with optimiz\$5) and (716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout )) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))))	USPAT; EPO; JPO; DERWENT	2003/05/13 10:57
-	10	clock and ((logic\$4 with optimiz\$5) and (716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3)) ) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout )) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))))	USPAT; EPO; JPO; DERWENT	2003/05/14 13:16